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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,184	12/10/2001	Jeroen Anton Johan Leijten	NL 000681	1259

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EXAMINER	
GERSTL, SHANE F	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,184	LEIJTEN ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE f this communication appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 have been examined.

Papers Received

2. Receipt is acknowledged of amendment papers filed where the papers have been placed of record in the file.

3. The amendment has successfully overcome the specification objections, however objections to the declaration and drawings remain as set forth below.

Oath/Declaration

4. The oath or declaration filed 04 March 2002 is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> Non-initialed and/or non-dated alterations have been made to the oath or declaration. See 37 CFR 1.52(c).

In this case, in the declaration filed 04 March 2002, the residence and post office address information for Mr. Bink has been altered but the alterations have not been initialed.

Drawings

5. The drawings are objected to because they do not indicate the proper headings as set forth in 37 CFR 1.121(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being

amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Tremblay et al (WO 00/33178).

8. In regard to claim 1, Tremblay et al discloses a signal processing device comprising

a. a plurality of functional units (UC1-UCn) (figure 5A, elements 520-526; figure 6, elements 620-626) for processing digital data based on an instruction word (figure 5C),

b. and a plurality of register files (RF1-RFn) for storing results obtained from respective ones of said functional units; [For several reasons the Examiner asserts that a plurality of register files is disclosed. First, the claim language simply states "a plurality of register files" but gives no indication of these being physically separate register files. The register segments of page 7, lines 18-25 include three "virtual register files" that contain replicated data for speed and area considerations. Second, figure 2 elements 224 and figure 5A elements 510-516, for example, both clearly show that the register segments may be separate register files. Third, the included IEEE standard definition of "register file" states that a register file is "a set of registers which may be addressed by their number in the set". Therefore, each of the replicated register segments or sets, which each have their own port and are thus separately addressable (as given above and in figures 2 and 5A, for example), are in fact register files.]

c. wherein said functional units are arranged to write a result to a predetermined register of said register files by using a register address (RRI) derived from said instruction word; [Figures 5A and 6 show that results are written to the register files via the line that returns to the register files from the functional units. Figure 5C along with page 12, lines 6-15 show that the instruction word specifies registers to use in the different register files (segments) using a certain number of bits, or an address (as described in the next paragraph of the reference).]

d. and register allocation means (RA) for selecting at least two of said register files (RF1-RFn) and for supplying said register address to said selected register files, if said instruction word comprises a corresponding indication. [Figure 3 and 5A and page 9, lines 25-30 show that the split register file (multiple register files) holds all the operands for instructions. The figure as well as the section of page 7 (replication) show that broadcast writes are performed to each register file and thus they are all selected for this write. As shown above, the instruction provides indication showing the register address to write to, which then corresponds to the broadcast write of multiple register files. The structure for this means is shown in the figures, where the register files receive the data and inherently the register index for this write to all of the register files, and thus is consistent with the structure given in the specification.]

9. In regard to claim 2, Tremblay et al discloses the device according to claim 1, wherein said functional units (UC1-UCn) are arranged to supply said corresponding indication to said register allocation means (RA). [Since the indication is the register address, the RA must receive the indication so the address of the broadcast write is known.]

10. In regard to claim 3, Tremblay et al discloses the device according to claim 1, wherein said signal processing device is a programmable VLIW processor (abstract), and said register files are partitioned register files (RF1-RFn), wherein a data stationary instruction encoding is used. [As shown above, the register file is split into 4 separate or partitioned register files. Figure 5C shows a data stationary instruction encoding

where the encoding of the instruction is stationary such that the encoding is fixed so that certain bits of data are always at certain locations in the word.]

11. In regard to claim 4, Tremblay et al discloses the device according to claim 1, wherein said corresponding indication is an information stating that said result is to be written to said register address of said selected register files (as shown above).

12. In regard to claim 5, Tremblay et al discloses the device according to claim 1, wherein said corresponding indication is a result index (RI) which refers to a multicast or broadcast register in said selected register files. [As shown above, the indication is an address or index to a broadcast register that is written to. Since this broadcast register is written to, the data to be written is inherently the result of some operation from a functional unit.]

13. In regard to claim 6, Tremblay et al discloses the device according to claim 1, wherein said register allocation means comprises demultiplexing means (DM1-DM3) for demultiplexing said result and said register address (RRI) to said selected register files in response to said corresponding indication. [As shown above, the register files receive a register address to write to and a result for writing to the address. Page 14, lines 22-23 show that the write ports of the register files receive data from the functional units including the result and the address or indicator. Page 15, lines 9-11 show that the write ports (for writing the result) comprise word lines for addressing a cell or register (also shown in page 14, lines 27-28) and bit lines for carrying the data (result). Thus the write port, which contains the result and address data, is demultiplexed into separate word and bit lines that contain the address and result, respectively.]

14. In regard to claim 7, Tremblay et al discloses the device according to claim 1, wherein said functional units are functional unit clusters (UC1-UCn). [Figures 5A and 6 show the functional units and that these units are grouped into a cluster. Another interpretation, would be to divide the functional units into two clusters, one cluster comprising elements 520 and 522 (or 620 and 622) and another cluster comprising elements 524 and 526 (or 624 and 626) and thus we have multiple functional unit clusters.]

15. In regard to claim 8, Tremblay et al discloses a method of supplying a signal processing result to a plurality of registers arranged in different register files (RA1-RAn) of a signal processing device (figure 5A, elements RF0-RF3; figure 6, elements 610-616), said method comprising the steps of:

a. determining a register address (RRI) based on an instruction word; [Figure 5C along with page 12, lines 6-15 show that the instruction word specifies registers to use in the different register files (segments) using a certain number of bits, or an address (as described in the next paragraph of the reference).]

b. supplying said register address to said plurality of register files, [The register address of above is inherently given to the register files so that the appropriate register is selected.]

c. and selecting said plurality of register files based on a corresponding indication in said instruction word and supplying said register address to said selected register files. [Figure 3 and page 9, lines 25-30 show that the split register file (multiple register files) holds all the operands for instructions. The

figure shows that broadcast writes are performed to each register file and thus they are all selected for this write. As shown above, the instruction provides indication showing the register address to write to, which then corresponds to the broadcast write of multiple register files.]

16. In regard to claim 9, Tremblay et al discloses the method according to claim 8, wherein said corresponding indication is an information stating that said result is to be written to said register address of said selected register files (as shown above).

17. In regard to claim 10, Tremblay et al discloses the method according to claim 8, wherein said corresponding indication is a result index (RI) which refers to a multicast or broadcast register in said selected register files (as shown above).

18. In regard to claim 11, Tremblay et al discloses the method according to anyone of claim 8, wherein said selection step comprises a demultiplexing step of demultiplexing said result and said register address to said selected register files in response to said corresponding indication. [As shown above, the register files receive a register address to write to and a result for writing to the address. Page 14, lines 22-23 show that the write ports of the register files receive data from the functional units including the result and the address or indicator. Page 15, lines 9-11 show that the write ports (for writing the result) comprise word lines for addressing a cell or register (also shown in page 14, lines 27-28) and bit lines for carrying the data (result). Thus the write port, which contains the result and address data, is demultiplexed into separate word and bit lines that contain the address and result, respectively.]

Response to Arguments

19. Applicant's arguments filed 10/27/04 have been fully considered but they are not persuasive.

20. Applicant has argued that Tremblay does not disclose a plurality of register files as set forth in claims 1 and 8, but instead discloses a single register file that is split into separate segments. For several reasons the Examiner maintains that a plurality of register files is disclosed. First, the claim language simply states "a plurality of register files" but gives no indication of these being physically separate register files. The register segments include three "virtual register files" that contain replicated data for speed and area considerations as given page 7, lines 18-25. Second, figure 2 elements 224 and figure 5A elements 510-516 both clearly show that the register segments may be separate register files. Third, the included IEEE standard definition of "register file" states that a register file is "a set of registers which may be addressed by their number in the set". Therefore, each of the replicated register segments or sets, which each have their own port and are thus separately addressable (as given above and in figures 2 and 5A, for example), are in fact register files.

21. Applicant next argues that Tremblay does not disclose register allocation means for selection at least to of said register files. Figures 3 and 5A and page 9, lines 25-30 show that the split register file (multiple register files) holds all the operands for instructions. The figure as well as the section of page 7 (replication) show that broadcast writes are performed to each register file and thus they are all selected (at least two) for this write. As shown above, the instruction provides indication showing the register address to write to, which then corresponds to the broadcast write of

multiple register files. The structure for this means is shown in the figures, where the register files receive the data and inherently the register index for this write to all of the register files, and thus is consistent with the structure given in the specification.

Conclusion

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

23. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
January 4, 2005

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